

Memory Performance Evaluation For Networking Applications

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Summary

Summary form only given. Memory performance evaluation of software applications running on contemporary processors is gaining importance with a growing gap between processor and memory performance. There are three well-known techniques used for memory performance evaluation and tuning: (1) source code analysis, (2) trace-driven simulation, and (3) measurements using on-chip counters especially in modern processor architectures for this purpose. We analyze the suitability of these methodologies to the memory performance evaluation of various network applications that are characterized by the requirement of delivering high throughput. Our observations indicate that none of the above three methods is effective in achieving high performance for networking applications. On the contrary, simple latency hiding techniques are very effective in obtaining high transaction throughput despite high memory overhead on contemporary processors.

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